REMARKS/ARGUMENT

Applicants' attorneys appreciate the Examiner's thorough search and remarks.

Responsive to the Examiner's requirement for a new oath or declaration, a new oath or declaration in compliance with 37 C.F.R. §1.67(a) is forthcoming.

Claim 1 has been canceled without prejudice and new claim 8 has been added to more particularly define applicants' invention. This amendment makes explicit what applicants believe was already implicit, and is, therefore, not made for purposes related to patentability.

Claim 1 is objected to due to informalities directed to whether the claimed channel region has a first or second conductivity type. New claim 8 clearly defines a plurality of spaced channel regions having a second conductivity type. Applicants respectfully submit that new claim 8 effectively overcomes the Examiner's objection.

Claims 1-7 stand rejected under 35 U.S.C. §112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. More particularly, the Examiner states it is not clear what is meant by "channels in the space between the peripheries of said channels and their respective sources." In response, new claim 8 excludes this allegedly indefinite language. It is now believed that claim 8 complies with 35 U.S.C. §112. Reconsideration is requested.

Dependent claims 2-7 depend directly or indirectly from independent claim 8, and are, therefore, patentable for the same reasons as well as because of the combination of features set forth in those claims with the features set forth in the claim(s) from which they depend.

Claims 1-3 stand rejected under 35 U.S.C. §103(a) as being obvious over Huang (U.S. Patent No. 6,255,692) in view of Lidow et al. (U.S. Patent No. 4,680,853). It was set forth that Huang shows each limitation of claim 1 except for a channel region of a second conductivity type. Applicants respectfully traverse this rejection.

The device shown in Huang comprises a trench type device that has vertically oriented invertible channel regions. Unlike the device shown in Huang, a device according to claim 8 comprises a plurality of *lateral invertible* channel regions. Applicants, therefore, respectfully submit that Huang does not teach or suggest a device according to claim 8.

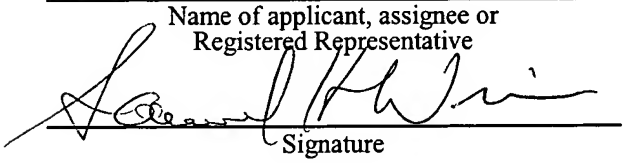
Claims 2-3 depend from claim 8, and are, therefore, patentable for the same reasons, as well as because of the combination of features set forth in claims 2 and 3 with the features set forth in claim 8. Reconsideration is requested.

Claims 4-7 depend indirectly from claim 8, and are, therefore, patentable for the same reasons, as well as because of the combination of features set forth in claim 8 with the features set forth in the claim(s) from which they depend. Reconsideration is requested.

The application is believed to be in condition for allowance. Such allowance is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Asst. Commissioner for Patents, Washington, D.C. 20231, on December 27, 2002:

Samuel H. Weiner
Name of applicant, assignee or Registered Representative



Signature

December 27, 2002
Date of Signature

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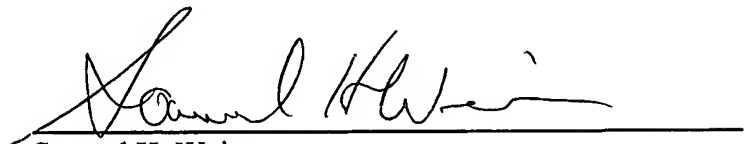
Respectfully submitted,



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APPENDIX A

"CLEAN" VERSION OF EACH PARAGRAPH/SECTION/CLAIM
37 C.F.R. § 1.121(b)(ii) AND (c)(i)

CLAIMS (with indication of amended or new):

2. (Amended) The MOSFET of claim 8, wherein said first and second conductivity types are N and P respectively.

3. (Amended) The MOSFET of claim 8, wherein said lateral invertible channels have a length of less than about 1 microns, whereby the distance between respective pairs of said source and channel regions at their corner points of maximum curvature is about 2.5 microns.

4. (Amended) The MOSFET of claim 8, which further includes a rectangular trench extending through the center of each of said plurality of source regions and into its respective channel region; and a high concentration contact diffusion of said first conductivity type disposed in the bottom of said trench; said source contact filling said trench and contacting said high concentration diffusion.

5. (Amended) The MOSFET of claim 2, which further includes a rectangular trench extending through the center of each of said plurality of source regions and into its respective channel region; and a high concentration contact diffusion of said first conductivity type disposed in the bottom of said trench; said source contact filling said trench and contacting said high concentration diffusion.

6. (Amended) The MOSFET of claim 3, which further includes a rectangular trench extending through the center of each of said plurality of source regions and into its respective channel region; and a high concentration contact diffusion of said first conductivity type disposed in the bottom of said trench; said source contact filling said trench and contacting said high concentration diffusion.

8. (NEW) A vertical conduction power MOSFET, comprising:

a die of monocrystaline silicon, said die being of a first conductivity type and having a first and a second surface;

a relatively thin layer of epitaxially grown silicon of said first conductivity type on said first surface;

a plurality of spaced channel regions of a second conductivity type diffused into the surface of said layer of epitaxially grown silicon;

a plurality of respective source diffusion regions of said first conductivity type, each of respective source diffusion regions being diffused into each of said plurality of spaced channel regions and each said respective source diffusion region having a smaller area than each of said plurality spaced channel regions, and defining at least one lateral invertible channel region in a space between its periphery of and its respective channel region;

a MOSgate structure overlying each of said lateral invertible channel regions;

a source electrode overlying a surface of said die and connected to each of said plurality of spaced channel regions and said respective source diffusion regions, and insulated from said MOSgate structure; and

a drain electrode coupled to said layer of epitaxially grown silicon, wherein each of said plurality of spaced channel regions has a depth of less than 3 microns, and each of said respective source diffusion regions has a depth of less than 0.3 microns.

APPENDIX B

VERSION WITH MARKINGS TO SHOW CHANGES MADE
37 C.F.R. § 1.121(b)(iii) AND (c)(ii)

CLAIMS:

2. (Amended) The MOSFET of claim [1] 8, wherein said first and second conductivity types are N and P respectively.

3. (Amended) The MOSFET of claim [1] 8, wherein said lateral invertible channels have a length of less than about 1 microns, whereby the distance between respective pairs of said source and channel regions at their corner points of maximum curvature is about 2.5 microns.

4. (Amended) The MOSFET of claim [1] 8, which further includes a rectangular trench extending through the center of each of said plurality of source regions and into its respective channel region; and a high concentration contact diffusion of said first conductivity type disposed in the bottom of said trench; said source contact filling said trench and contacting said high concentration diffusion.

5. (Amended) The MOSFET of claim 2, which further includes a rectangular trench extending through the center of each of said plurality of source regions and into its respective channel region; and a high concentration contact diffusion of said first conductivity type disposed in the bottom of said trench; said source contact filling said trench and contacting said high concentration diffusion.

6. (Amended) The MOSFET of claim 3, which further includes a rectangular trench extending through the center of each of said plurality of source regions and into its respective channel region; and a high concentration contact diffusion of said first conductivity type disposed in the bottom of said trench; said source contact filling said trench and contacting said high concentration diffusion.

APPENDIX C
COMPLETE SET OF "CLEAN" CLAIMS
PURSUANT TO 37 C.F.R. §1.121(C)(3)

2. The MOSFET of claim 8, wherein said first and second conductivity types are N and P respectively.

3. The MOSFET of claim 8, wherein said lateral invertible channels have a length of less than about 1 microns, whereby the distance between respective pairs of said source and channel regions at their corner points of maximum curvature is about 2.5 microns.

4. The MOSFET of claim 8, which further includes a rectangular trench extending through the center of each of said plurality of source regions and into its respective channel region; and a high concentration contact diffusion of said first conductivity type disposed in the bottom of said trench; said source contact filling said trench and contacting said high concentration diffusion.

5. The MOSFET of claim 2, which further includes a rectangular trench extending through the center of each of said plurality of source regions and into its respective channel region; and a high concentration contact diffusion of said first conductivity type disposed in the bottom of said trench; said source contact filling said trench and contacting said high concentration diffusion.

6. The MOSFET of claim 3, which further includes a rectangular trench extending through the center of each of said plurality of source regions and into its respective channel region; and a high concentration contact diffusion of said first conductivity type disposed in the bottom of said trench; said source contact filling said trench and contacting said high concentration diffusion.

7. The MOSFET of claim 5, wherein said first concentration type is N and wherein said high concentration contact diffusion is a phosphorus diffusion formed with an effective implant energy of greater than about 350 keV for a singly charged phosphorous ion.

8. A vertical conduction power MOSFET, comprising:

a die of monocrystaline silicon, said die being of a first conductivity type and having a first and a second surface;

a relatively thin layer of epitaxially grown silicon of said first conductivity type on said first surface;

a plurality of spaced channel regions of a second conductivity type diffused into the surface of said layer of epitaxially grown silicon;

a plurality of respective source diffusion regions of said first conductivity type, each of respective source diffusion regions being diffused into each of said plurality of spaced channel regions and each said respective source diffusion region having a smaller area than each of said plurality spaced channel regions, and defining at least one lateral invertible channel region in a space between its periphery of and its respective channel region;

a MOSgate structure overlying each of said lateral invertible channel regions;

a source electrode overlying a surface of said die and connected to each of said plurality of spaced channel regions and said respective source diffusion regions, and insulated from said MOSgate structure; and

a drain electrode coupled to said layer of epitaxially grown silicon, wherein each of said plurality of spaced channel regions has a depth of less than 3 microns, and each of said respective source diffusion regions has a depth of less than 0.3 microns.